ECE4250 Lab 5 Report

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# Objective

This lab’s objective was to create a binary coded decimal (BCD) counter to get experience with sequential processes in VHDL. In this case, a single digit BCD counter was created based on the given conditions and table.

# Lab Work

Using Figure 2-46 from the textbook as an example, I made the BCD counter according to the input conditions provided. Input bits are LOAD, ENABLE, and UP which are all synchronous, and CLR which is asynchronous. LOAD is set when loading a new value into the counter. ENABLE is set to make the counter function, otherwise nothing happens regardless of other bits. UP is set for incrementing count, otherwise the counter decrements. CLR resets the counter values to 0 when set. The counter is rising edge triggered, and sets the output to the current stored value, then increments the stored value. Since it is a single digit decimal counter, 4 bits are used for the value and one carry bit is used to indicate when going from 9 to 0 on increment, or 0 to 9 on decrement.

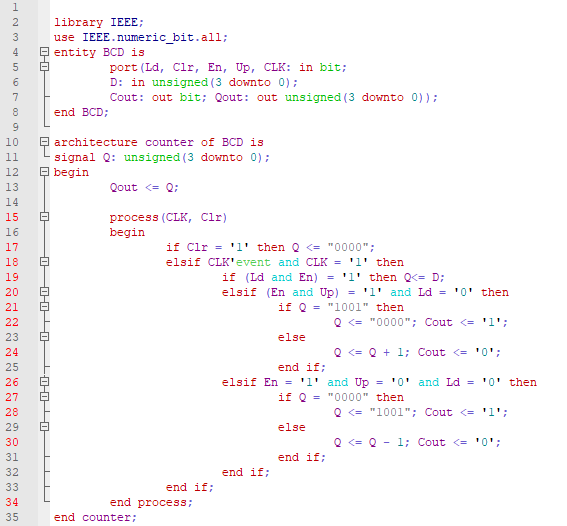


Figure . Counter code

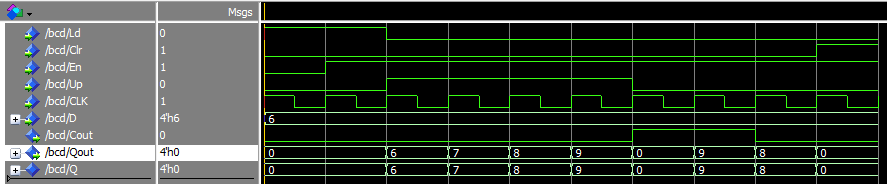


Figure . Counter Simulation

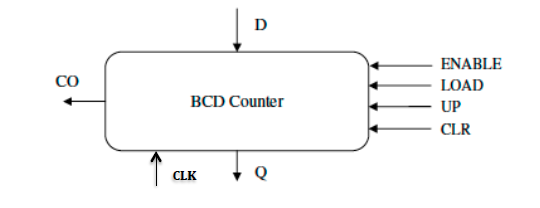


Figure . Counter block diagram

# Questions

1. after step 2, increment the counter 4 times, Co is 1 since the output is going from 9 to 0.
2. When counter is 0 and UP = 0, the next state is 9 with Co = 1 since the counter will decrement from 0. In this case, Co is really indicating a borrow, but since it is a single digit, it is just indicating the rollover state.

# Conclusion

This lab was a good introduction to sequential processes using a counter. Using the book example made implementation straightforward, but I had some issues with ordering of if statements. Initially I had checking CLR bit inside the clock tick, which caused delays in clearing. After fixing that and getting variable names to matched up, the program worked as expected.

Reference:

C. H. Roth, L. K. John. “Introduction to VHDL,” in *Digital System Design Using VHDL*. 3rd Ed. Boston MA, United States: Cengage, 2016, ch. 2.